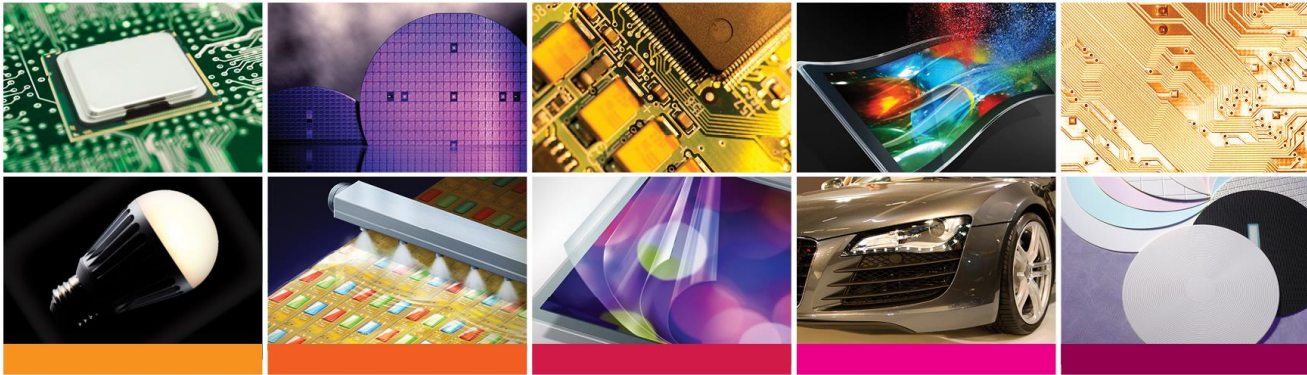




## Electronic Materials



# INTERLINK™ 9200 Cu TSV

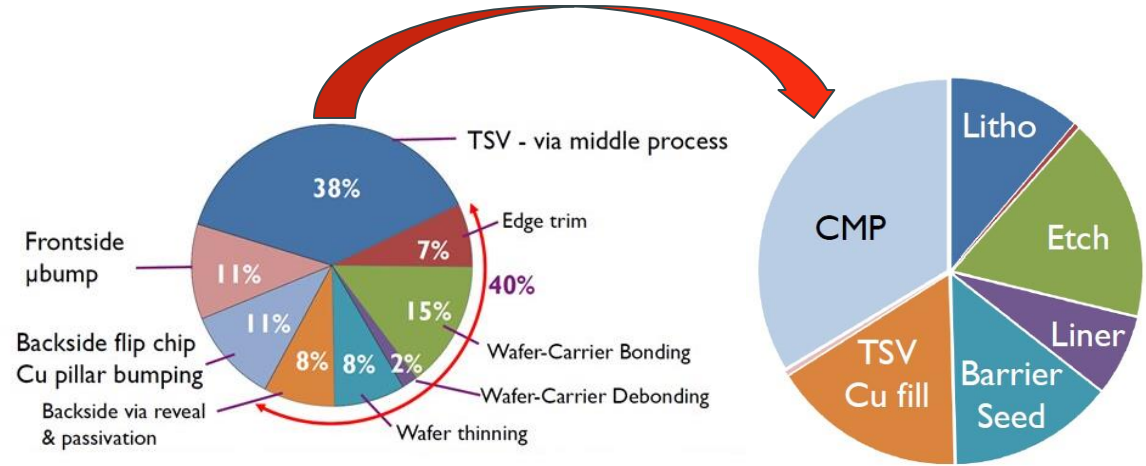
Advanced Packaging Technologies

# Outline

- Introduction: TSV for 2.5D and 3D Packaging
- INTERLINK™ 9200 Cu TSV
  - ❑ Formulation
  - ❑ Mechanism of bottom-up fill Cu deposition
- Segment Plating Results
  - ❑ 5x55 µm via-middle
  - ❑ 10x100 µm via-last
  - ❑ High aspect ratio – next-generation devices
- 300 mm Plating Results
- INTERLINK™ 9200 Process Window and Stability
- Conclusions

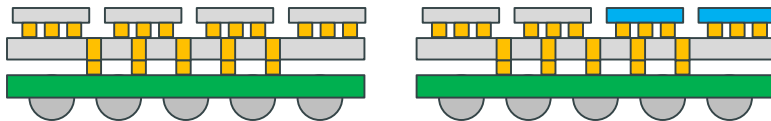
# Introduction: TSVs for 2.5D and 3D Packaging

- High performance devices
- Low latency between dies
- Maximum I/O density
- Decreased power consumption
- High costs for CMP and via filling



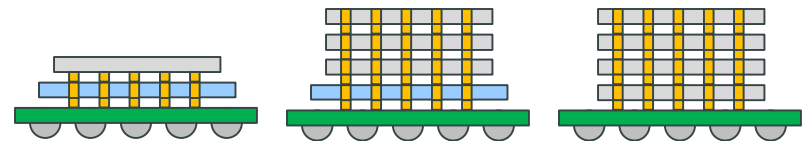
## Interposers: 2.5D

- Able to use existing die layouts
- Can combine high yield die processes already in place
- Bridge to true 3D design



## Die-stacking: 3D

- New die design layout/rules needed
- Smallest device layout, highest performance



**— INTERLINK™ 9200 Cu TSV**

# INTERLINK™ 9200 Cu TSV

## Formulation

INTERLINK™ 9200 Cu TSV Formulation (For Catholyte Chamber)			
Product Name	Function	Target	Range
INTERLINK™ 9200 Accelerator	De-polarizer, accelerates Cu plating & allows bottom-up fill	3 mL/L	2.5 – 3.5 mL/L
INTERLINK™ 9200 Suppressor	Polarizer that slows Cu plating and provides wetting of vias	6 mL/L	2 – 8 mL/L
INTERLINK™ 9200 Leveler	Sidewall polarizer, slows rate of Cu plating	3.5 mL/L	3 – 4 mL/L
INTERLINK™ 9200 Electrolyte	Source of Cu ions, provides pH adjustment and bath conductivity	60 g/L Cu <sup>2+</sup> ; 10 g/L H <sub>2</sub> SO <sub>4</sub> ; 80 ppm Cl <sup>-</sup>	Cu <sup>2+</sup> : +/- 5%; Acid, Cl <sup>-</sup> : +/- 10%

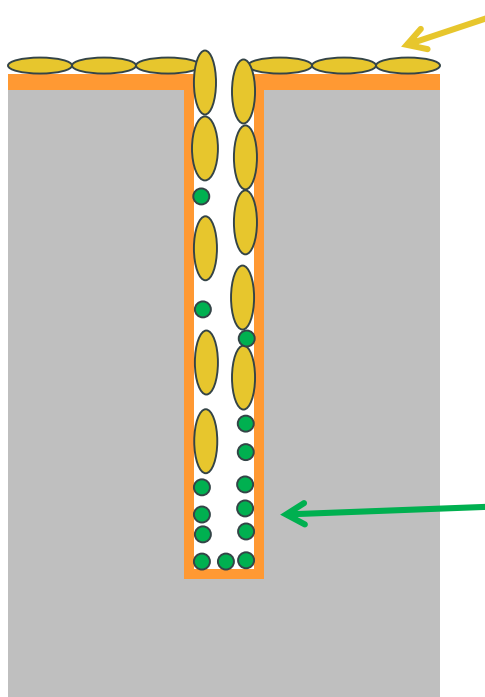
INTERLINK™ 9200 Cu TSV Formulation (For Anolyte Chamber)			
Product Name	Function	Target	Range
INTERLINK™ 9200 Anolyte	Electrolyte designed to work with Cu anode in the Anolyte Chamber	60 g/L Cu <sup>2+</sup> ; 0.3 g/L H <sub>2</sub> SO <sub>4</sub> ; 80 ppm Cl <sup>-</sup>	Cu <sup>2+</sup> : +/- 5%; Acid, Cl <sup>-</sup> : +/- 10%

- INTERLINK™ 9200 Cu TSV uses a 3-component additive system (Accelerator, Suppressor, Leveler), with membrane in the plating cell, to deposit Cu in 2.5D & 3D TSV packaging applications
- Additive components specially formulated to allow for rapid, defect-free bottom up filling performance within 10x100 μm and 5x50 μm TSV features
- Target dosing can be modified to achieve optimized performance on a specific wafer type and pattern layout



# INTERLINK™ 9200 Cu TSV

## *Mechanism of Bottom-up Fill*



### Suppressor:

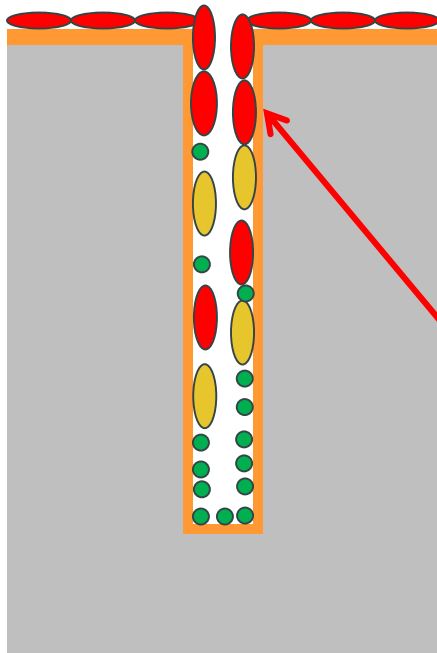
- Used to lower surface tension of plating bath, allowing proper wetting of TSV vias and wafer surface, reducing surface defects
- Weaker suppressor preferred to allow stronger polarizing leveler to polarize via sidewalls
- Suppressor also can compete with accelerator adsorption to the surface, supporting the leveler and offering additional Cu deposition control

### Accelerator:

- Needed to initiate bottom-up filling at via bottom
- Relatively low dosing needed to maintain bath stability
- Higher doses needed for rapid via filling
- Dosing set by balance between stability and plating rate

# INTERLINK™ 9200 Cu TSV

## *Mechanism of Bottom-up Fill*



### **Leveler:**

- Used to polarize field area as well as via sidewalls
- Strong polarizing leveler used to minimize Cu deposition on wafer field area and on upper via sidewalls
- Leveler required to prevent plating defects such as pinch-off voids and surface nodules
- Too strong of leveler causes doping of deposited Cu, surface defects, as well as preventing top of via filling

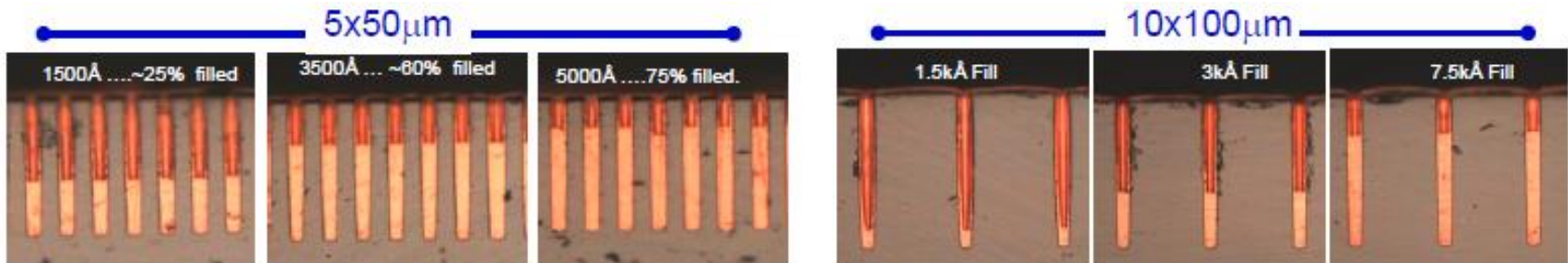
# **INTERLINK™ 9200 Segment Plating Results**



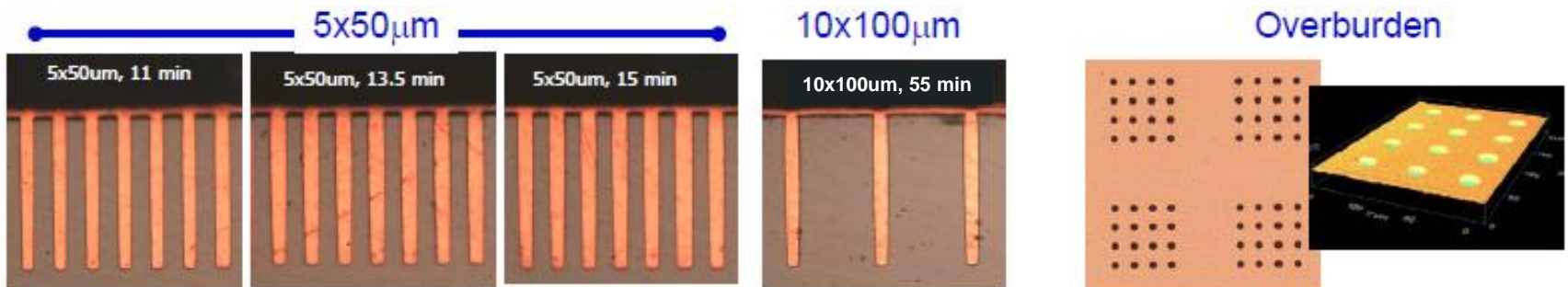
# INTERLINK™ 9200 Segment Plating Results

## Partial and Full Fill on 5x55 μm and 10x100 μm Test Wafers

- Partial Filling Sequences: Strong polarization at via opening → ideal filling profile



- Via filling speed tests: Rapid filling capability
  - ❑ Plating Cycle times ~15 min (5x50 μm), and ~55 min (10x100 μm) demonstrated in segment level test (wafer dependent)
- Full Filling Sequences: Low overburden thickness, smooth deposits



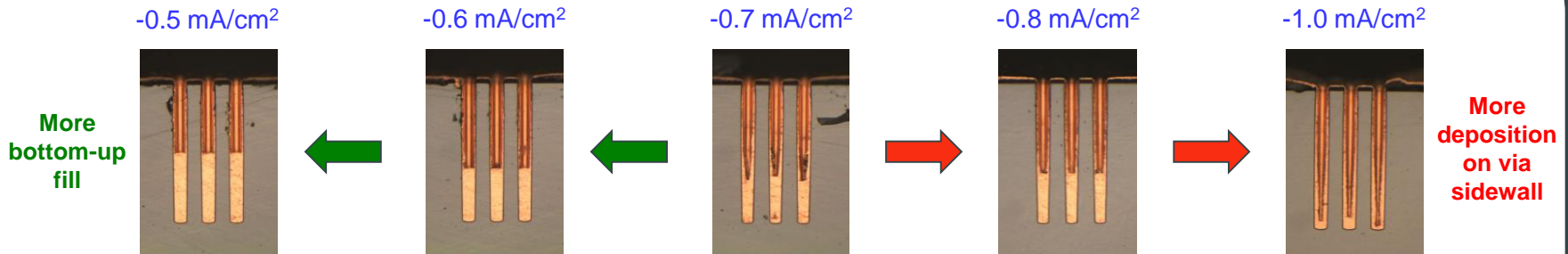
0.80μm OB for 1.5μm Cu deposit  
 $R_a \leq 10\text{nm}$



# INTERLINK™ 9200 Segment Plating Results

## Initial Plating Rate and Full Fill Void Inspection

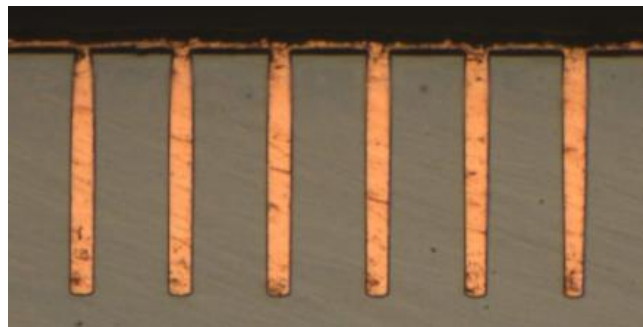
### Bottom-up Fill Initiation: Impact of 1<sup>st</sup> plating step CD



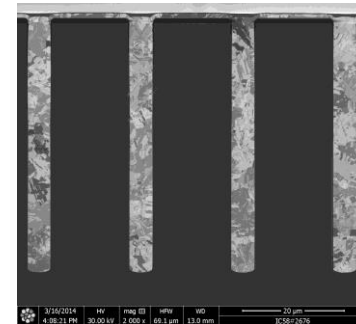
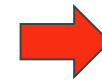
- Plating initiated with slower CD step allows for improved bottom-up fill
- Plating too fast initially does not allow enough time for Cu diffusion to bottom of the via
- Balance of Additive concentration and plating waveform to optimize fill time/performance

### Full Fill Study: FIB-SEM Confirmation of Void-free Plating

4-step waveform  
16.4 minutes  
60-10-80 Electrolyte  
3/6/3.5 mL/L {A/S/L}



5x55 µm TSV Features

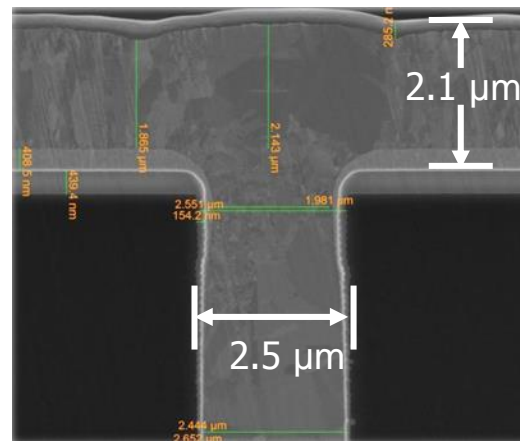


Void-Free!

# INTERLINK™ 9200 Segment Plating Results

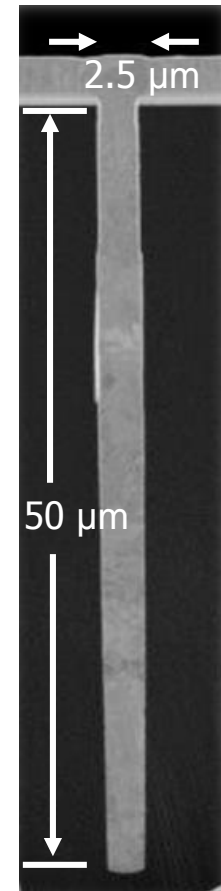
## *Extension to Next-Generation Applications*

- INTERLINK™ 9200 can be extended into future generation applications including TSV features with an aspect ratio of 20:1 (2.5x50  $\mu\text{m}$ )
- Bottom-up fill is maintained with challenging aspect ratio, TSV vias are void-free as confirmed by FIB-SEM
- Cu plating still occurs mostly in-via, with minimal overburden



Images provided courtesy of Applied Materials

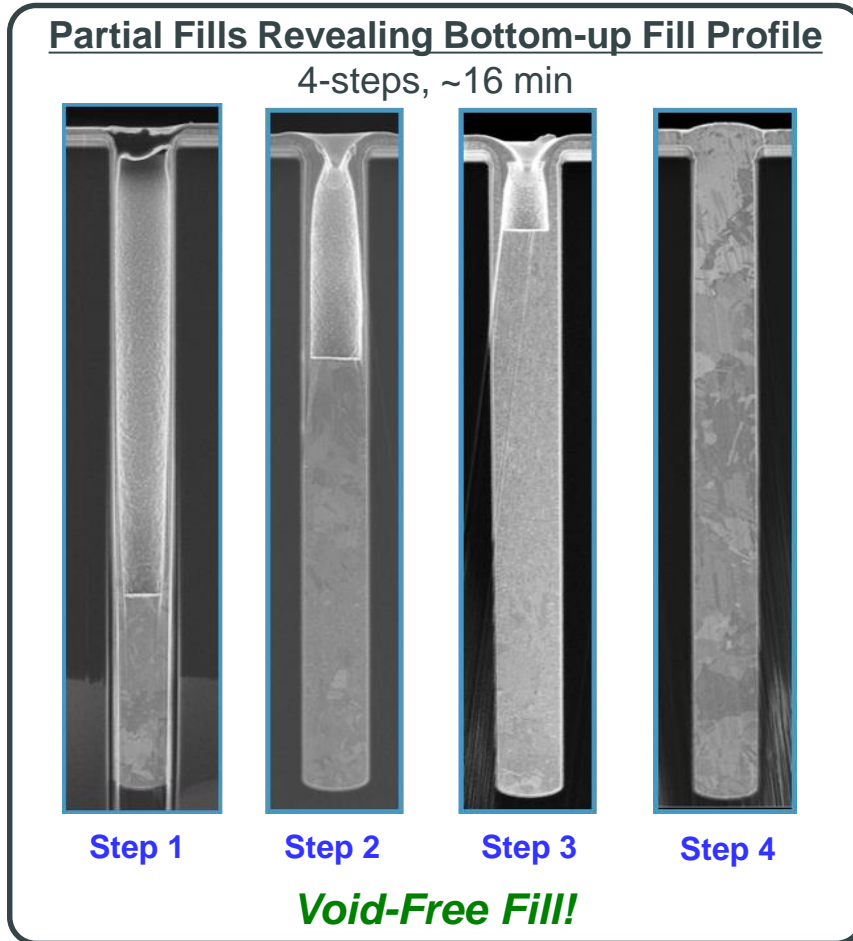
4-step plating waveform  
Void-free fill



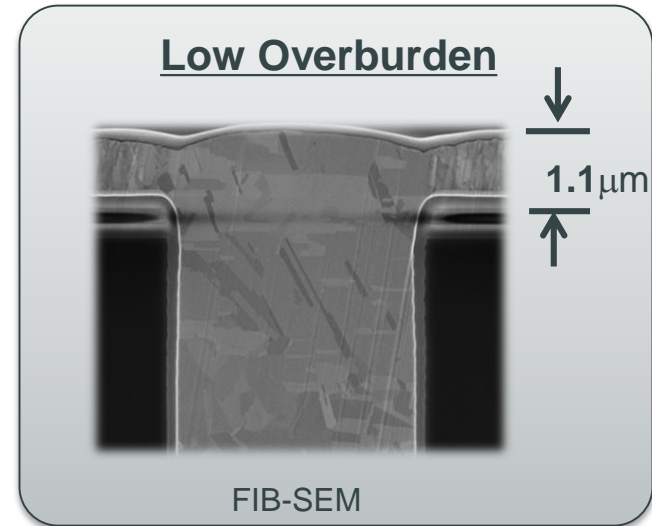
# **INTERLINK™ 9200: 300 mm Plating Results**

# INTERLINK™ 9200: 300 mm Plating Results

## Partial and Full Fill on 5x55 μm Test Wafers



*Images provided courtesy of Applied Materials*

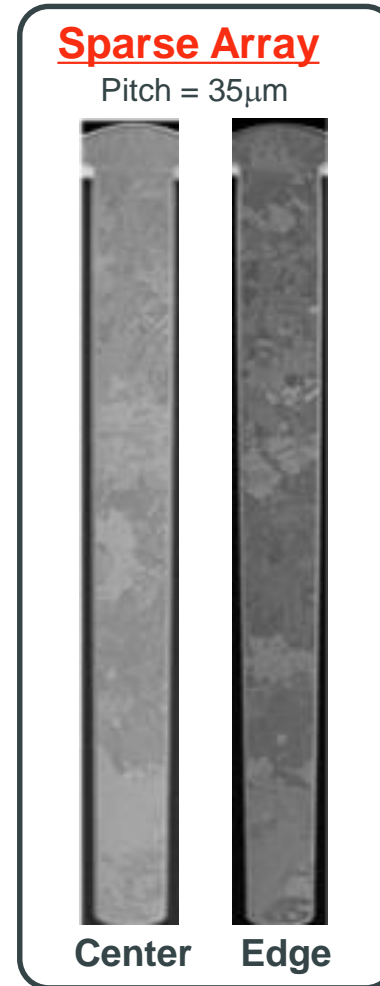
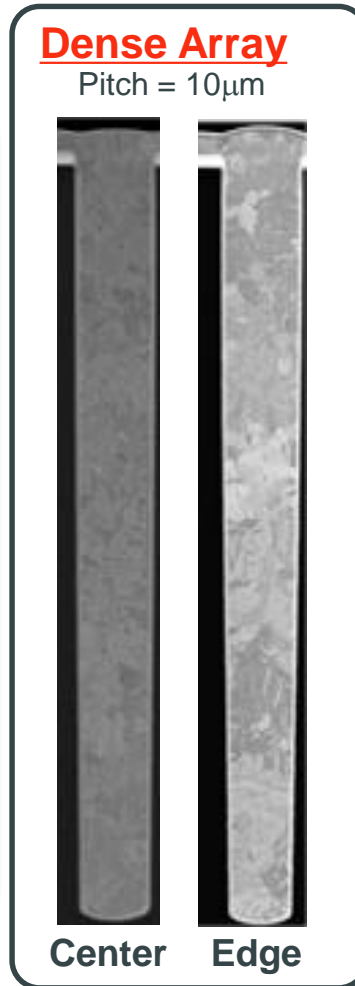


- Strong sidewall suppression during deposition prevents voiding at the top of the via
- Low total overburden of ~1 μm minimizes CMP processing
- Fill times of less than 20 min.

# INTERLINK™ 9200: 300 mm Plating Results

## Center-to-Edge Effects on 5x55 μm Test Wafers

- Uniform plating overburden from center to edge of wafers
- Same via filling rates independent of via pitch, allowing for flexible die layout
- Small changes in via over-bump with pitch, minimizing CMP issues



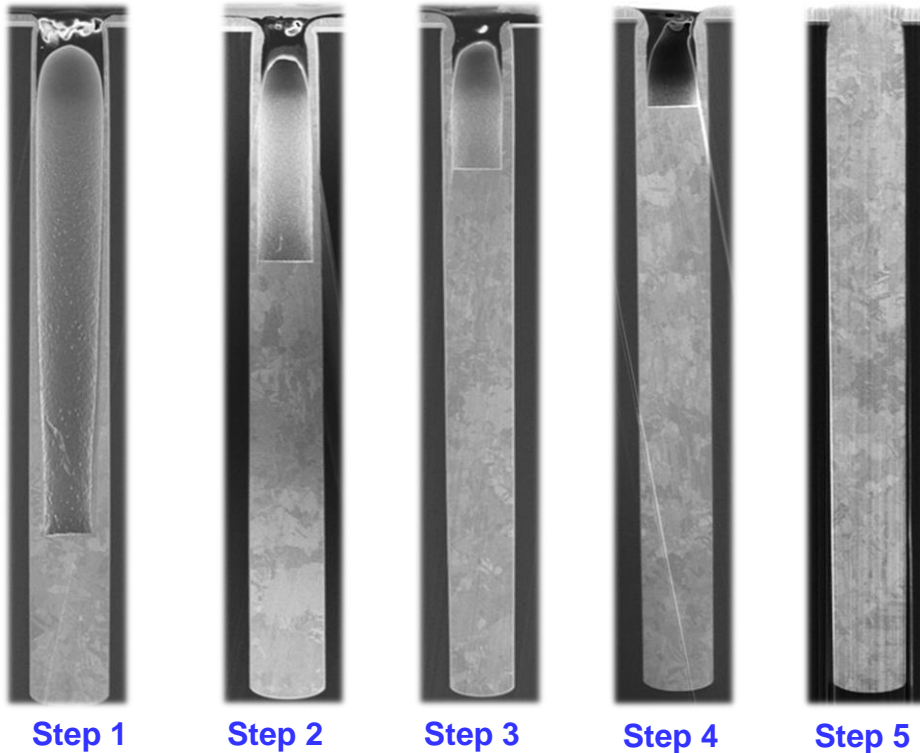
*Images provided courtesy of Applied Materials*

# INTERLINK™ 9200: 300 mm Plating Results

## Partial and Full Fill on 10x100 μm Test Wafers

### Partial Fills Revealing Bottom-up Fill Profile

5-steps, ~55 min



**Void-Free Fill!**

*Images provided courtesy of Applied Materials*

### Low Overburden



- Bottom-up filling with strong suppression of sidewalls and via opening
- Minimal overburden of ~1.5-2 μm reduces CMP processing time
- Fill times of less than 60 min. achieved

# **INTERLINK™ 9200 Process Window and Stability**



# INTERLINK™ 9200 Process Window and Stability

## 5x55 μm Test Wafer at Segment Level

		[Accelerator]		
		-25 %	Target	+25%
[Leveler]	-25%			
	Target			
	+25%			

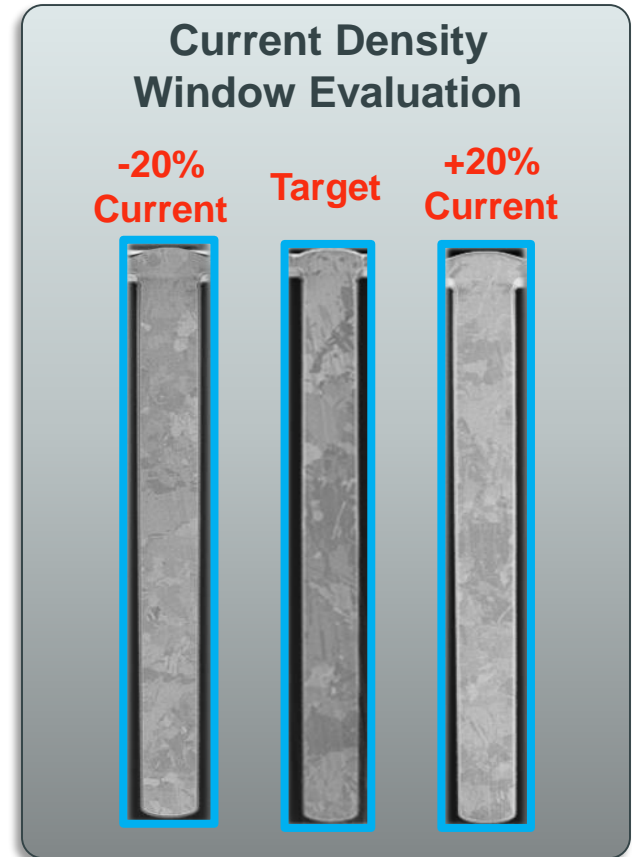
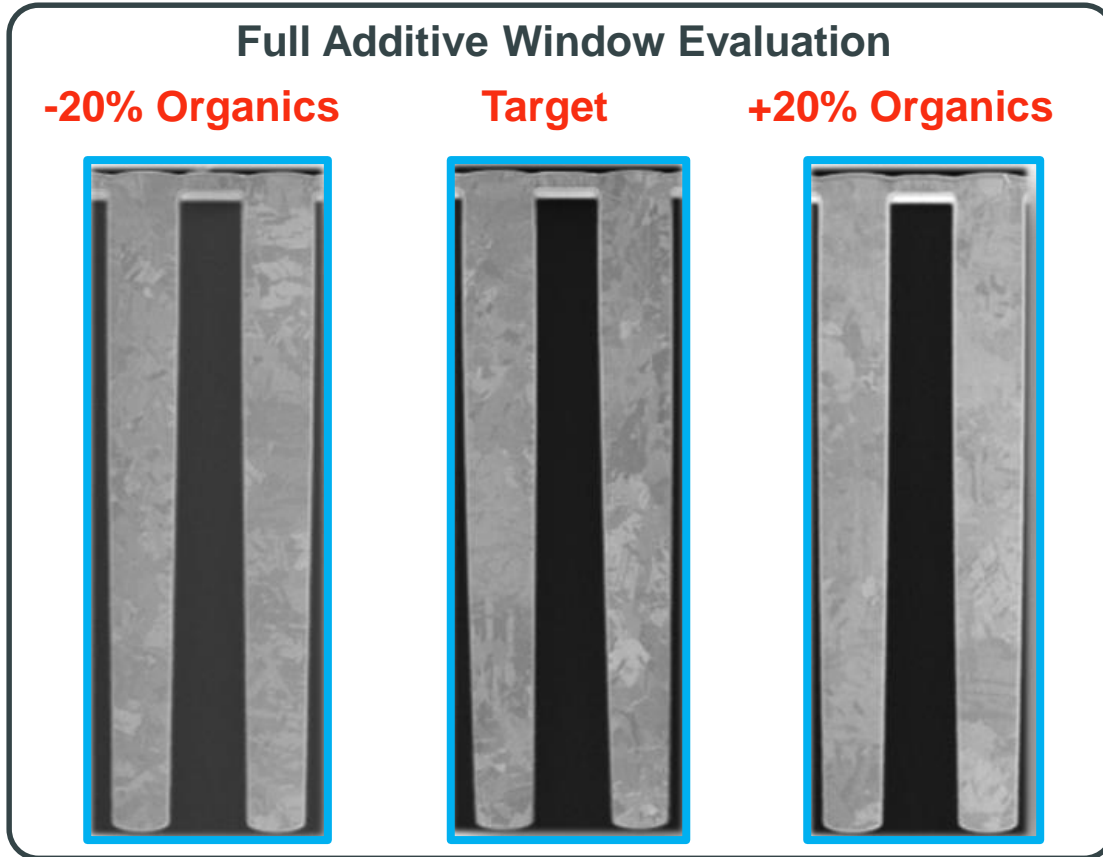
- Aggressive filling time enables better centering of chemistry dosing
- Target leveler dosing exhibits void-free full filling with wide accelerator window
- Low leveler content exhibits voiding at via bottoms – not enough sidewall polarization

- 4 step plating cycle
- 16.5 min. fill time

Membrane segment plater, 700 mL catholyte chamber, 1 L anolyte chamber

# INTERLINK™ 9200 Process Window and Stability

## 5x55 μm Test Wafer at Tool Level

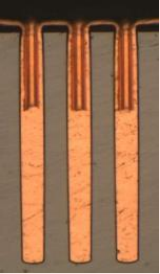
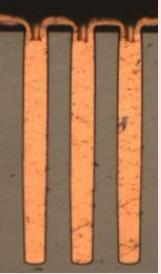

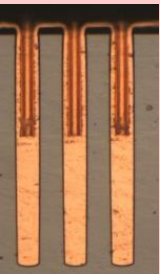
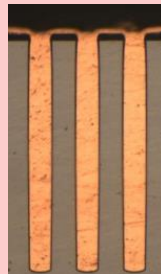
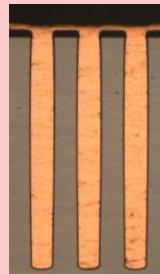
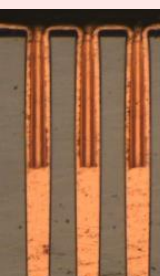




*Images provided courtesy of Applied Materials*

➤ INTERLINK™ 9200 displays a wide additive and current density process window

# INTERLINK™ 9200 Process Window and Stability

## 10x100 μm Test Wafer at Segment Level

		[Accelerator]		
		-66 %	Target	+66%
[Leveler]	-42%			
	Target			
	+42%			

- Increased accelerator content within a leveler dosing increases fill rate
- Increased leveler content slows fill speeds and increases time for full fill
- Target dosings give rapid void-free filling of vias

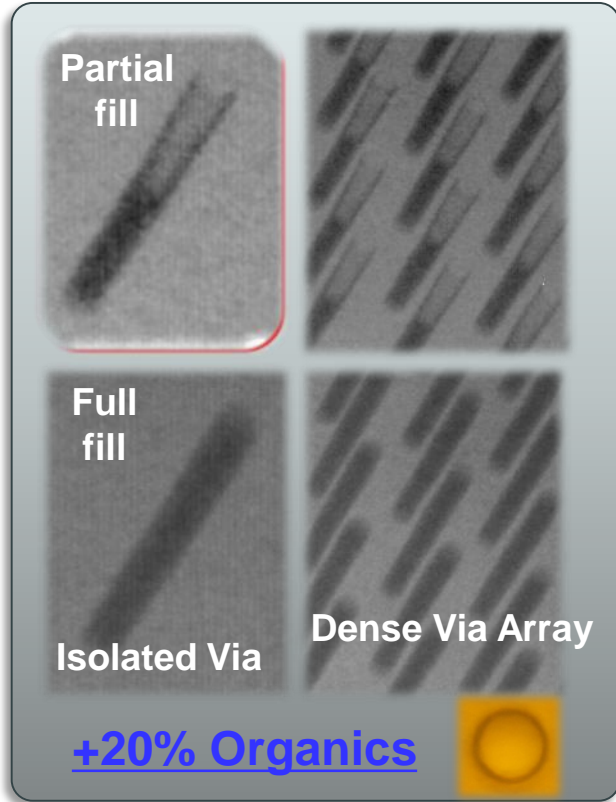
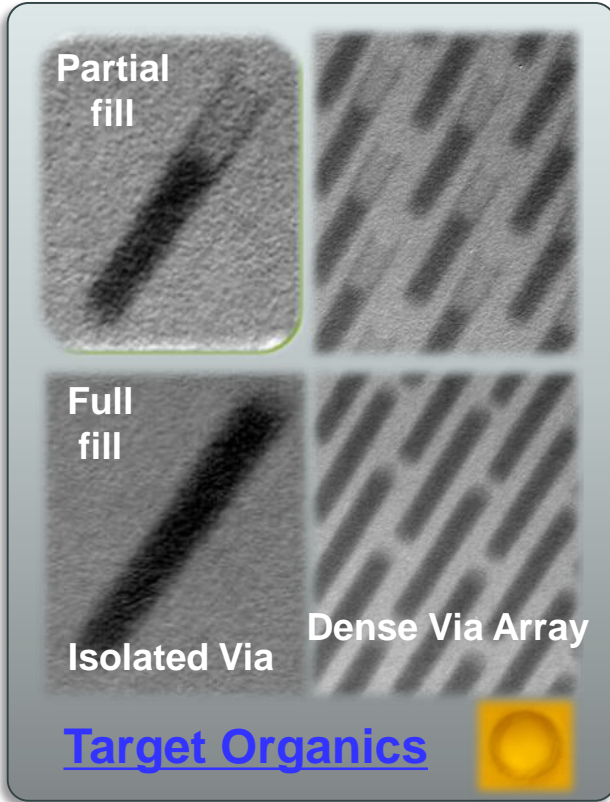
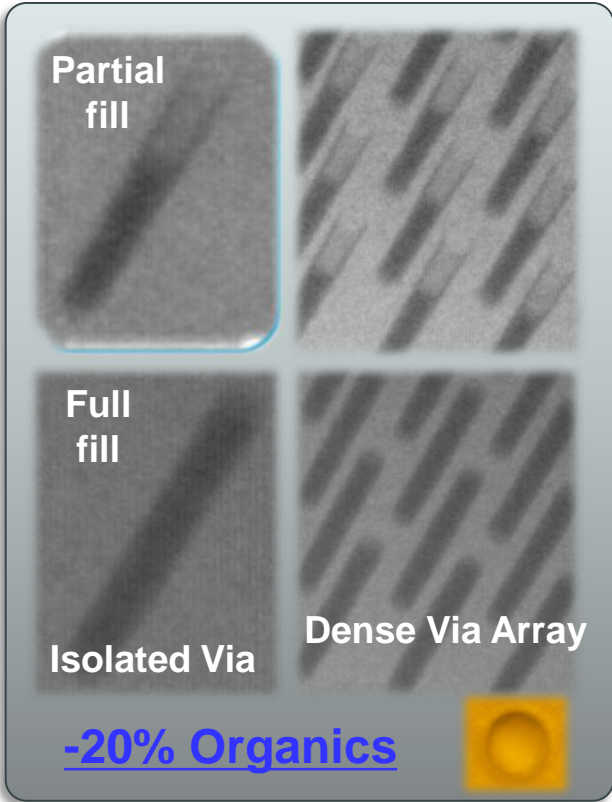
- 4 step plating cycle
- 56 min. fill time

Membrane segment plater, 700 mL catholyte chamber, 1 L anolyte chamber



# INTERLINK™ 9200 Process Window and Stability

10x100 μm Test Wafer at Tool Level



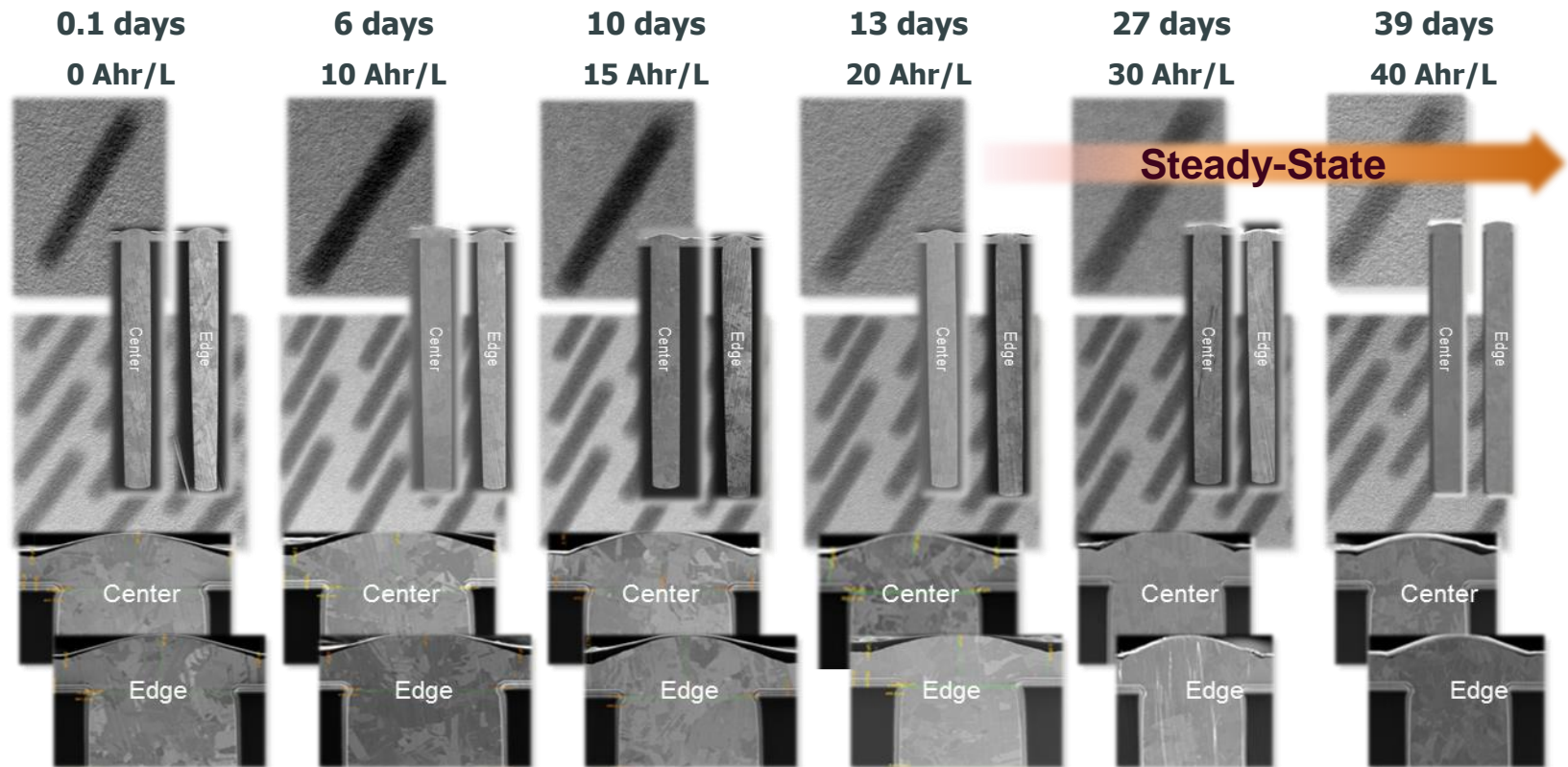
Images provided courtesy of Applied Materials

- Void-free filling with a wide  $\pm 20\%$  organic dosing window
- Similar fill speeds between via pitches across dosing window

# INTERLINK™ 9200 Process Window and Stability

## Fill Performance Throughout Electrolytic Aging

### 10 × 100 μm Via Filling Stability



Images provided courtesy of Applied Materials

- Greater than 40 Ahr L<sup>-1</sup> bath life with both 10 × 100 μm and 5 × 50 μm vias
- Equivalent of ~10,000 5 × 50 μm wafers or ~4,000 10 × 100 μm wafers



## Conclusions

- INTERLINK™ 9200 was developed to provide fast bottom-up fill of Cu into TSV features of 10x100 μm down to 5x50 μm and 2.5x50 μm
- Fill times of ~55 min for 10x100 μm features and ~16 min for 5x50 μm features achieved at the 300 mm tool level
- INTERLINK™ 9200 has shown a wide process window of ±20% for both the additives and the plating rate
- INTERLINK™ 9200 shows stable plating performance at the 300 mm tool level up to 40 Ahr/L





**Thank  
You**